REMARKS

Claims 14-18 have been indicated as allowed. Claims 9 and 13 have been objected to as being dependent on a rejected base claim.

The noted informalities of Claims 6 and 9 have been addressed.

Claims 1-8 and 10-12 were rejected under 35 U.S.C. 102(b) as being anticipated by Hirose.

Claim 1 has been amended to recite "means for programming at least one of the complementary MOS transistors in the first/second inverter adapted for causing, after programming, an irreversible degradation of a gate oxide layer of that at least one MOS transistor." The Examiner points to non-volatile devices 13 and 13' in Hirose. These devices 13/13', however, are not MOS transistors which are "in the first/second inverter" as claimed. Rather, the non-volatile devices 13/13' are shown in Hirose Fig. 1 as being located outside of the inverters 14/14'. Applicants further note that the claimed irreversible degradation occurs with respect to one of the transistors of the inverter. In Hirose, that would equate to one of transistor 10/10' or transistor 11/11'. However, in Hirose the data is permanently stored using non-volatile transistors 13/13' connected between the inverters, rather than using degradation of the inverter transistors as claimed. In view of the foregoing, Applicants respectfully submit that claim 1, as amended, defines over Hirose. Allowance of claim 1, and its dependent claims, is requested.

Turning next to claim 10, Applicants respectfully traverse the rejection and assert that the Examiner has failed to properly consider claim language which defines over Hirose. In claim 10, Applicants claim "a pair of load transistors connected to a reference voltage." The Examiner correctly identifies Hirose transistors 10/10'. Applicants still further claim that "the

programming circuit [delivers] a voltage to the gate of the at least one load transistor which is sufficient to cause an irreversible gate oxide degradation of the load transistor for purposes of programming the memory cell to permanently store a certain data value." Thus, what Applicants claim is that it is one of the load transistors which is programmed through gate oxide degradation. This structure and operation is neither disclosed nor suggested by Hirose with respect to the load transistors 10/10'. It is clear from Hirose col. 5, line 22 to col. 6, line 26 that NO gate degradation operation is performed with respect to the load transistors 10/10'. Rather, non-volatile elements 13/13' are connected between the inverters 14/14' for the purpose of changing the timing with which the input of one inverter is coupled to the output of the other inverter (col. 5, lines 63-67). The characteristics of the gate oxides of the load transistors 10/10' are not changed by the operation of the transistors 13/13'. Allowance of claim 10, and its dependent claims, is respectfully requested.

New Claims 21-22 are asserted to be define over Hirose because there is no teaching or suggestion for the use of series connected programming transistors as claimed.

Respectfully submitted,
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